Abstract – This report describes the readout electronics that will be used for the silicon strip detector array to be installed at the ELI-NP facility.

ELECTRONIC CASE

The readout of the silicon strip detector array will be performed by using the Generic Electronics for TPCs (GET). This would ensure high resolution keeping costs low and strongly reducing the bulk of the front end electronics. Research and development activity would be necessary to adapt the GET electronics to X3 and QQQ3 silicon strip detectors. In particular, external preamplifiers have to be implemented to guarantee the best energy and position resolution and proper coupling with the GET readout.

An additional advantage of the adoption of a GET systems is the possibility to have common electronics and DAQ systems with other experiments to be installed at the ELI-NP facility, leading to a standardization of the readout systems strongly enhancing the efficiency of the setups.

GET ELECTRONICS

The GET project is an international collaborative effort to investigate a novel approach towards building medium sized scalable system with a presently maximum of 30k channels having multiple possible applications with comparatively high throughput capabilities and resolution. The choice of new technological solutions allows a reduction in the number of point-to-point connections in the system and should therefore provide for a more reliable system. A fully computerized and distributed control approach will give fast calibration and significant reduction in the set-up time of the system [1].

The core component of the GET electronics is a custom-made 64-channel ASIC chip called AGET (ASIC for GET) that employs Switched Capacitor Array (SCA) fast analog memory. The block diagram of the AGET chip is displayed in Fig.1.

Four AGET chips are mounted on a single front-end AsAd card (ASIC and ADC). Its main features are the following:

- SCA analog, circular buffers with 512 cells (sampling points) per channel;
- adjustable sampling frequency of SCA buffers (1 – 100 MHz);
- 12-bit ADC with dynamic range of 2 V$_{p-p}$ and with fixed sampling frequency of 25 MHz for reading SCA memories (one ADC channel per AGET chip);
- possibility to bypass charge- and/or shaping amplifier;
- self- and external triggering, hit counting and test pulse injecting capabilities.

Figure 1: Block diagram of the AGET chip

The global view of the GET electronic is displayed in fig. 2:

Figure 2: Global view of the GET electronic
The digital outputs of the 4 ADCs are transmitted by 8 differential lines with a maximum speed of 1.2 Gbit/s to the CoBo board.

The CoBo (Concentration Board) board is responsible for applying a time stamp, zero suppression and compression algorithms to the data. It will also serve as a communication intermediary between the AsAd and the outside world. The slow control signals and commands to the AsAd will be transmitted via the CoBo (four AsAD per CoBo).

The Mutant (Multiplicity Trigger And Time) card manages the multiplicity, the conditions for the trigger, and the distribution of the clock on the whole system. The global data is transmitting through network switch to computer farm.

CoBo and MuTanT are set in microTCA crate [2]. Data are transmitted through a 10 Gb-Ethernet network to the computer farm. A µTCA chassis can houses ten CoBos and a MUTANT.

The BEM (Back-End Module) card must ensure the interface between the GET electronics and other ancillary equipment used in nuclear physics experiments.

Taking into account that the use to charge-partition silicon strip detectors, proposed for ELI-NP facility, allows us to reduce to 311 the number of channels to be instrumented, it means that two boards would be necessary to handle the whole detector readout. R&D activity is presently ongoing to achieve high position and energy resolution using X3 and QQQ3 detectors, with respect to preamplifiers and readout software. A major aim is to achieve pulse shape discrimination in the case of charge partition position sensitive silicon detectors.

REFERENCES